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EXAMINER	
EWART, JAMES D	

ART UNIT	PAPER NUMBER
2683	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/839,514	STRUHSAKER ET AL.	
	Examiner	Art Unit	
	James D. Ewart	2683	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *04-19-2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Objections

1. Claim 1 is objected to because of the following informalities: the claim recites "at least one of one or more additional cards" and should be "at least one or more additional cards" . Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1,2,4,5,7,10,11,12,14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable by Williams et al (EP 0 849 684 A) and further in view of Garnett (U.S. Patent No. 6,262,493).

Referring to claim 1, Williams et al discloses a system for the on-line insertion of a line replaceable unit (Column 1, Lines 18-20 & 51-54 and Column 10, Lines 25-27) into a backplane (Column 4, Lines 20-29 and Column 5, Lines 25-28) of an item of electronic equipment wherein said backplane comprises a common control bus (Column 5, Line 29-31), one or more operational buses (Figure 5, Vcc) and one or more traffic buses (Column 2, Lines 5-19), said system comprising: a primary master controller inserted into said backplane (Column 1, lines 46-57 and Column 5, Line 29-30 and Figure 1, 22), said primary master controller capable of communicating via said common control bus of said backplane with said line replaceable unit

when said line replaceable unit is inserted into said backplane (Column 4, Lines 24-33 and Column 8, Lines 18-35); wherein said line replaceable unit does not have full access to all buses in said backplane when said line replaceable unit is first inserted into said backplane (Column 3, Lines 44-47, Column 4 Lines 24-33 and Column 8, Lines 18-35); and wherein said primary master controller is capable of causing said line replaceable unit to have full access to remaining buses in said backplane (Column 5, Line 21 and Column 8, Lines 18-35), but does not teach one or more additional control buses and wherein a line replaceable unit is partially powered and does not have access to full power until full power is provided. Garnett teaches one or more additional control buses (Column 1, Line 67 to Column 2, Line 4) and wherein a line replaceable unit is partially powered and does not have access to full power until full power is provided (Column 12, Lines 19-37). Therefore at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to combine the teaching of Williams et al with the teaching of Garnett teaches one or more additional control buses and wherein a line replaceable unit is partially powered and does not have access to full power until full power is provided to improve fault identification and/or diagnosis for a field replaceable unit.

Referring to claim 11, Williams et al discloses for use in association with a backplane of an item of an electronic equipment wherein said backplane comprises a common control bus (Column 5, Line 29-31), one or more operational buses (Figure 5, Vcc) and one or more traffic buses (Column 2, Lines 5-19), a method for the on-line insertion for of an electronic line replaceable unit into a backplane (Column 1, Lines 18-20 & 51-54 and Column 10, Lines 25-27) said method comprising the steps of: inserting a primary master controller into said backplane

(Column 1, lines 46-57, Figure 1, 22 and Column 5, Lines 29-30); inserting said line replaceable unit into said backplane so that said line replaceable unit does not have full access to all buses in said backplane (Column 4 Lines 24-33, Column 3, Lines 44-47 and Column 8, Lines 18-35); and controlling the access of said line replaceable unit to remaining buses in said backplane with said primary master controller (Column 3, Lines 44-47, Column 4 Lines 24-33 and Column 8, Lines 18-35), but does not teach one or more additional control buses and wherein a line replaceable unit is partially powered and does not have access to full power until full power is provided. Garnett teaches one or more additional control buses (Column 1, Line 67 to Column 2, Line 4) and wherein a line replaceable unit is partially powered and does not have access to full power until full power is provided (Column 12, Lines 19-37). Therefore at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to combine the teaching of Williams et al with the teaching of Garnett teaches one or more additional control buses and wherein a line replaceable unit is partially powered and does not have access to full power until full power is provided to improve fault identification and/or diagnosis for a field replaceable unit.

Referring to claims 2 and 12, Williams et al further discloses wherein said primary master controller is capable of determining whether said line replaceable unit that is inserted into said backplane is ready for operation (Column 4, lines 48-53).

Referring to claims 4 and 14, Williams et al further discloses wherein said primary master controller is capable of causing said line replaceable unit to have access to full power in said backplane (Column 4, Lines 34-40).

Referring to claims 5 and 15, Williams et al further discloses wherein said primary master controller comprises an interface control processor card (Column 1, Lines 55-57 and Column 4, Line 29), and wherein said line replaceable unit comprises a circuit board card (Column 2, Lines 35-39).

Referring to claim 7, Williams et al further discloses wherein said primary master controller is capable of disconnecting full access of said line replaceable unit to said backplane after said primary master controller has caused said line replaceable unit to have full access to said backplane (Column 6, Lines 17-28).

Referring to claim 10, Williams et al further teaches a circuit board card capable of being inserted into said backplane (Column 5, Lines 29-36), said circuit board card comprising a hot swap power/in rush controller for regulating power to said circuit board card when said circuit board card is first inserted into said backplane (Column 1, Lines 49-57 and Column 8, Lines 18-35); and a card processor on said circuit board card said card processor capable of determining whether said circuit board card is located in a non-master controller slot of said backplane (Column 8, Lines 18-35), in which case said circuit board card waits for said primary master

controller to cause said circuit board card to have full access to said backplane (Column 8, Lines 18-35).

3. Claims 3 and 13 are rejected under 35 USC 103(a) as being unpatentable over Williams et al and Garnett and further in view of Lysik et al (U.S. Patent No. 5,754,785).

Referring to claims 3 and 13, Williams et al and Garnett teach the limitations of claims 3 and 13, but do not teach wherein said controller is capable of downloading at least one software update to said line replaceable unit to cause said line replaceable unit to be ready for operation. Lysik et al teaches wherein said controller is capable of downloading at least one software update to said line replaceable unit to cause said line replaceable unit to be ready for operation (Column 2, Lines 52-58). Therefore, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to combine the art of Williams et al and Garnett with the teaching of Lysik et al wherein said controller is capable of downloading at least one software update to said line replaceable unit to cause said line replaceable unit to be ready for operation to provide a system which conducts a substantially non-disruptive upgrade of communications network equipment (Column 1, Lines 36-39).

4. Claims 6, 9, and 16 are rejected under 35 USC 103(a) as being unpatentable over Williams et al and Garnett and further in view of Gerhart et al. (EP 0 460 307).

Referring to claims 6 and 16, Williams et al and Garnett teach the limitations of claims 6 and 16, but do not teach a secondary master controller inserted into said backplane, said secondary master controller capable of performing the functions of said primary master controller when said primary master controller is not operating. Gerhart et al. teaches a secondary master controller inserted into said backplane, said secondary master controller capable of performing the functions of said primary master controller when said primary master controller is not operating (Page 4, Lines 24-30). Therefore, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to combine the art of Williams et al and Garnett with the teaching of a secondary master controller inserted into said backplane, said secondary master controller capable of performing the functions of said primary master controller when said primary master controller is not operating so that the secondary controller can assume the primary status when the primary controller is not operational (Page 4, Lines 28-30).

Referring to claim 9, Williams et al teaches the limitations of claim 9, including a circuit board card capable of being inserted into said backplane, said circuit board card comprising a hot swap power/in rush controller for regulating power to said circuit board card when said circuit board card is first inserted into said backplane and a card processor on said circuit board card (Column 1, Lines 49-57) but does not teach; wherein said card processor is capable of determining whether said circuit board card is located in a primary master controller slot of said backplane , in which case said circuit board card operates as a primary master controller; and wherein said card processor is capable of determining whether said circuit board card is located

in a secondary master controller slot of said backplane, in which case said circuit board card operates as a secondary master controller when said primary master controller is not operating. Gerhart et al. teaches, wherein said card processor is capable of determining whether said circuit board card is located in a primary master controller slot of said backplane (Page 4, Lines 28-30), in which case said circuit board card operates as a primary master controller (Page 4, Lines 28-30); and wherein said card processor is capable of determining whether said circuit board card is located in a secondary master controller slot of said backplane in which case said circuit board card operates as a secondary master controller when said primary master controller is not operating (Page 4, Lines 28-30). Therefore at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to combine the art of Williams et al and Garnett with the teaching of Gerhart et al. wherein said card processor is capable of determining whether said circuit board card is located in a primary master controller slot of said backplane, in which case said circuit board card operates as a primary master controller; and wherein said card processor is capable of determining whether said circuit board card is located in a secondary master controller slot of said backplane in which case said circuit board card operates as a secondary master controller when said primary master controller is not operating so that the secondary controller can assume the primary status when the primary controller is not operational (Page 4, Lines 28-30).

5. Claims 8 and 17 are rejected under 35 USC 103(a) as being unpatentable over Williams et al and Garnett and further in view of Gupta et al. (U.S. Patent No. 5,996,083).

Referring to claims 8 and 17, Williams et al and Garnett teach the limitations of claims 8 and 17, but do not teach wherein said primary master controller is capable of disconnecting full access of said line replaceable unit to said backplane by disabling power to all but common control power sections of said line replaceable unit. Gupta et al teaches wherein said primary master controller is capable of disconnecting full access of said line replaceable unit to said backplane by disabling power to all but common control power sections of said line replaceable unit (Column 1, Lines 17-32 and Column 4, Lines 5-7). Therefore, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to combine the art of Williams et al and Garnett with the teachings of Gupta et al wherein said primary master controller is capable of disconnecting full access of said line replaceable unit to said backplane by disabling power to all but common control power sections of said line replaceable unit to reduce power consumption (Column 1, Line 20).

6. Claim 18 is rejected under 35 USC 103(a) as being unpatentable over Williams et al in view of Tavallaei (EP 0 898 231 A) and in further view of Garnett.

Referring to claim 18, Williams et al teaches a backplane (Column 5, Line 21) of an item of electronic equipment wherein said backplane comprises a common control bus (Column 5, Line 29), one or more operational buses (Figure 5, Vcc) and one or more traffic buses (Column 2, Lines 5-19), a method for the on-line insertion of a line replaceable unit into said backplane (Column 4, Lines 20-29 and Column 5, Lines 25-28), said method comprising the steps of: inserting a circuit board card into said backplane (Column 4, Lines 20-29 and Column 5, Lines

25-28), but does not teach providing a controlled power ramp up to said circuit board card; determining whether a voltage rail has failed; starting a reset timer; running a power on self test on said circuit board card; determining whether said circuit board card passed said power on self test; and activating a common control bus. Tavallaei teaches providing a controlled power ramp up to said circuit board card (Column 12, Lines 36-38); determining whether a voltage rail has failed (0017 and Column 12, Line 39); starting a reset timer (Column 12, line 38); running a power on self test on said circuit board card (Column 12, Line 39); determining whether said circuit board card passed said power on self test; and activating a common control bus (Column 12, lines 39-42). Therefore at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to combine the art of Williams et al with the teaching of Tavallaei teaches providing a controlled power ramp up to said circuit board card; determining whether a voltage rail has failed; starting a reset timer; running a power on self test on said circuit board card; determining whether said circuit board card passed said power on self test; and activating a common control bus to continue operation with little or no down time (0007). Williams et al and Tavallaei teach the limitations of claim 18, but do not teach one or more additional control buses. Garnett teaches one or more additional control buses (Column 1, Line 67 to Column 2, Line 4). Therefore at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to combine the teaching of Williams et al and Tavallaei with the teaching of Garnett teaches one or more additional control buses to improve fault identification and/or diagnosis for a field replaceable unit.

Referring to claim 20, Williams et al teaches said method further comprising the steps of: determining that said circuit board card is not in a master slot of said backplane (Column 8, Lines 18-35); waiting for a primary master controller to interrogate said circuit board card (Column 8, Lines 18-35); configuring said circuit board card with said primary master controller; activating said circuit board card with said primary master controller; and operating said circuit board card in normal operation (Column 8, Lines 18-35).

7. Claim 19 is rejected under 35 USC 103(a) as being unpatentable over Williams et al, Tavallaei, and Garnett and further in view of Gehart et al.

Referring to claim 19, Williams et al, Tavallaei, and Garnett teach the limitations of claim 19, but do not teach determining whether said circuit board card is in a master slot of said backplane; determining whether said circuit board card is a primary master controller if said circuit board card is in a master slot of said backplane; operating said circuit board card as a primary master controller if said circuit board card is a primary master controller; determining whether said circuit board card is a secondary master controller if said circuit board card is in a master slot of said backplane; and operating said circuit board card as a secondary master controller if said circuit board card is a secondary master controller. Gerhart et al. teaches determining whether said circuit board card is in a master slot of said backplane; determining whether said circuit board card is a primary master controller if said circuit board card is in a master slot of said backplane (Page 4, Lines 28-30); operating said circuit board card as a primary master controller if said circuit board card is a primary master controller (Page 4, Lines

28-30); determining whether said circuit board card is a secondary master controller if said circuit board card is in a master slot of said backplane; and operating said circuit board card as a secondary master controller if said circuit board card is a secondary master controller (Page 4, Lines 28-30). Therefore at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to combine the art of Williams et al with the teaching of determining whether said circuit board card is in a master slot of said backplane; determining whether said circuit board card is a primary master controller if said circuit board card is in a master slot of said backplane; operating said circuit board card as a primary master controller if said circuit board card is a primary master controller; determining whether said circuit board card is a secondary master controller if said circuit board card is in a master slot of said backplane; and operating said circuit board card as a secondary master controller if said circuit board card is a secondary master controller so that the secondary controller can assume the primary status when the primary controller is not operational (Page 4, Lines 28-30)

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to James D. Ewart whose telephone number is (571) 272-7864. The examiner can normally be reached on M-F 7am - 4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William Trost can be reached on (571)272-7872. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)305-3900.

Ewart
June 2, 2005

WILLIAM TROST
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